IN THE SPECIFCIATION

Please insert the following new paragraph at page 1, line 1 of the specification.

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Cross-Reference to Related Application

The present application is a continuation of U.S. Patent Application Serial No. 09/432,526, now issued as U.S. Patent No. 6,681,341, which was filed on November 3, 1999, by William Fredenburg et al.

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Please replace the paragraph at page 6, lines 22-23 with the following amended version thereof.

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Fig 6. is a schematic block diagram of a row synchronization logic circuit of the IHB;

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Please replace the paragraph at page 9, line 23 to page 10, line 10 with the following amended version thereof.

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The processing engine 300 comprises a plurality of symmetrically arrayed processing elements (PE) 400. In the embodiment shown in Fig. 3, the processing engine comprises four (4) rows and four (4) columns symmetrically arrayed in a 4 x 4 configuration between an input header buffer (IHB) 500 and an output header buffer (OHB) 900. However it should be noted that other configurations, such as a 6 x 6 arrayed configuration or similar rectangularly arrayed configurations, may be advantageously used with the present invention. A 64-bit feedback path 350 couples the OHB 900 to the IHB 500 and provides a data path for recycling data through the PE stages of the processing engine. The PEs of each row are configured as stages connected in series by a 100 MHz 64-bit direct memory access (DMA) data path 340 that synchronously transfers data and control "context" from one PE to the next. Specifically, the processing elements of each row are configured as stages of a pipeline that sequentially execute operations on the transient data loaded by the IHB 500, whereas the processing elements of each column operate in parallel to perform substantially the same operation on the transient data, but with a shifted phase. An example of an arrayed processing engine and network switch suitable for use with the present invention is described in copending and commonly-owned US Patent Application Serial No. 09/106,478, now issued as U.S. Patent No. 6,513,108, titled *Programmable Arrayed Processing Engine Architecture for a Network Switch.*

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